In the Claims:

Claims 1-3 (Canceled).

4. (Previously presented) An integrated search engine device, comprising:

a content addressable memory (CAM) core that is configured to support at least one database of searchable entries therein; and

a control circuit that is configured to generate at least one signal at an output of the search engine device in response to detecting a done status of at least one of a plurality of result status signals that indicate states of completion of a corresponding plurality of contexts being handled by the search engine device;

wherein the at least one signal comprises an aggregate result status signal having a leading edge that is synchronized with a transition of a result status signal when the transition indicates completion of a first-to-finish one of the plurality of contexts being handled by the search engine device during overlapping time intervals.

5. (Original) The device of Claim 4, wherein said control circuit comprises combinational logic that is configured to maintain the aggregate result status signal in an active state so long as a value of any one of the plurality of result status signals indicates a state of completion of a respective one of the plurality of contexts.

6. (Original) The device of Claim 4, wherein said control circuit further comprises:

a plurality of context specific result mailboxes that are configured to store return values associated with corresponding ones of the plurality of contexts; and

a result status register that is configured to store done status values associated with the plurality of contexts.

7. (Original) The device of Claim 6, wherein the search engine device is configured to support a maximum number N of contexts; and wherein said result status register comprises N single-bit storage devices.

8. (Original) The device of Claim 7, wherein the search engine device further comprises a memory mapped interface that is coupled to an M-bit wide data bus; and wherein a value of N/M equals a positive integer greater than one.

Claims 9-24 (Canceled).

25. (Previously presented) An integrated search engine device, comprising:

a memory mapped interface; and

a control circuit electrically coupled to said memory mapped interface, said control circuit configured to generate an aggregate result status signal at an output of said memory mapped interface in response to detecting a done status of at least one of a plurality of result status signals, which indicate states of completion of a corresponding plurality of contexts being handled by the search engine device;

wherein the control circuit is configured so that the aggregate result status signal has a leading edge that is synchronized with a transition of a result status signal when the transition indicates completion of a first-to-finish one of the plurality of contexts being handled by the search engine device during overlapping time intervals.

26. (Original) The device of Claim 25, wherein said control circuit comprises combinational logic that is configured to maintain the aggregate result status signal in an active state so long as a value of any one of the plurality of result status signals indicates a state of completion of a respective one of the plurality of contexts.

27. (Original) The device of Claim 25, wherein said control circuit further comprises:

a plurality of context specific result mailboxes that are configured to store return values associated with corresponding ones of the plurality of contexts; and

a result status register that is configured to store done status values associated with the plurality of contexts.

28. (Original) The device of Claim 27, wherein the search engine device is configured to support a maximum number N of contexts; and wherein said result status register comprises N single-bit storage devices.

29. (Original) The device of Claim 28, wherein the search engine device further comprises a quad data rate interface that is coupled to an M-bit wide data bus; and wherein a value of N/M equals a positive integer greater than one.

Claims 30-43 (Canceled).

44. (Previously presented) A packet coprocessor chip, comprising:

a control circuit that is configured to generate at least one signal at an interface of the coprocessor chip in response to detecting a done status of at least one of a plurality of result status signals that indicate states of completion of a corresponding plurality of contexts being handled by the coprocessor chip; and

wherein the at least one signal comprises an aggregate result status signal having a leading edge that is synchronized with a transition of a result status signal when the transition indicates completion of a first-to-finish one of the plurality of contexts being handled by the coprocessor chip during overlapping time intervals.

45. (Original) The chip of Claim 44, wherein said control circuit comprises combinational logic that is configured to maintain the aggregate result status signal in an active state so long as a value of any one of the plurality of result status signals indicates a state of completion of a respective one of the plurality of contexts.

46. (Original) The chip of Claim 44, wherein said control circuit further comprises:

a plurality of context specific result mailboxes that are configured to store return values associated with corresponding ones of the plurality of contexts; and

a result status register that is configured to store done status values associated with the plurality of contexts.